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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/099,754	03/14/2002	Michael J. Peters	00939s-050510US	9162

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EXAMINER	
SAXENA, AKASH	

ART UNIT	PAPER NUMBER
2128	

DATE MAILED: 06/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/099,754	PETERS ET AL.	
	Examiner	Art Unit	
	Akash Saxena	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 March 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) *4-7,11 and 12* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3, 8-10, 13-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 March 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/14/02 1/20/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-3, 8-10, 13-17 have been presented for examination based on the application filed on 14th March 2002.
2. Claims 4-7 and 11-12 are cancelled based on amendment filed on 14th March 2002.

Priority

3. This application appears to be a division of Application No. 08/299395, filed 1st September 1994, now U.S. Patent 6,480,817 (Issued 12th Nov. 2002). A later application for a distinct or independent invention, carved out of a pending application and disclosing and claiming only subject matter disclosed in an earlier or parent application is known as a divisional application or "division." The divisional application should set forth the portion of the earlier disclosure that is germane to the invention as claimed in the divisional application.

Claim Objections

4. Claim 15 is objected to as it discloses phrase "at least two response values" for the first mode of operation and "at least three response values" for the second mode of operation. These references to the bidirectional pad model are vague and do not clarify which response values are being referred to. Although, examiner interprets these values for "at least two response values" as the input & output signals and "at least three response values" as input, output & resolved signals, nevertheless objections are made to request clarification in the claim language.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 5,428,800 issued to Wen-Jai Hsieh et al (Hsieh '800 hereafter).

Regarding Claim 1

Hsieh '800 teaches a system for bi-directional signal transfer system (Hsieh '800: Abstract Lines 1-3; Col.2, Lines 26-28; Figure 4). Hsieh '800 teaches means for maintaining an input value though the use of buffers (Hsieh '800: Col.2, Lines 29-32, Figure 4: From 76 to 108 & From 70 to 110). Hsieh '800 teaches means for maintaining the output though the use of buffer/isolation circuit (Hsieh '800: Fig.4 Elements 100 & 104 or 102 & 106). Hsieh '800 teaches means for generating the third value based on input (first value) & output (second value) as output from the one shot device (Hsieh '800: Elements 104 or 102).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,428,800 issued to Wen-Jai Hsieh et al (Hsieh '800 hereafter) in view of U.S. Patent No. 5,202,593 issued to Thomas B. Huang et al (Huang '593 hereafter).

Regarding Claim 2

Hsieh '800 teachings are disclosed in claim 1 rejection above.

Hsieh '800 does not teach third value based on the resistor.

Huang '593 teaches means of generating third value based on resistive data (Huang '593: Figure 2: Element 102 to 110 to 104 (3rd output); Col.3 Lines 46-57), which according to the specification is derived from the pull up/pull down resistors/cells (Specification: Lines 24-27).

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of Huang '593 to Hsieh '800 to derive the third value based on the resistive data. The motivation would have been that since Hsieh '800 teaches using Huang '593 design (Col.1, Lines 19-20).

7. Claims 3,8 & 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,428,800 issued to Wen-Jai Hsieh et al (Hsieh '800 hereafter) in view of U.S. Patent No. 4,922,445 issued to Yoshito Mizoue et al (Mizoue '445 hereafter).

Regarding Claim 3

Hsieh '800 teachings are disclosed in claim rejection above.

Hsieh '800 does not teach storing the first, second & third values of the model to a computer file.

Mizoue '445 teaches storing the input (first value) as well as output (second & third) values to a computer file (Mizoue '445: Col.2, Lines 34-38, 50-59) during the simulation of a model.

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of Mizoue '445 to Hsieh '800 to store the value input/output/intermediate values of the simulated model. The motivation would have been that Mizoue '445 teaches a switch level simulator that works for bi-directional switches (Col.6, Lines 36-44) and Hsieh '800 is designing a bidirectional transfer system. Hence Mizoue '445 solves the modeling and capturing the input/intermediate/output state problem in Hsieh '800 model by modeling it through his simulator.

Regarding Claim(s) 8

Hsieh '800 teaches a system for bi-directional signal transfer system (Hsieh '800: Abstract Lines 1-3; Col.2, Lines 26-28; Figure 4). Hsieh '800 teaches means for

maintaining an input value though the use of buffers (Hsieh '800: Col.2, Lines 29-32, Figure 4: From 76 to 108 & From 70 to 110). Hsieh '800 teaches means for maintaining the output though the use of buffer/isolation circuit (Hsieh '800: Fig.4 Elements 100 & 104 or 102 & 106). Hsieh '800 teaches means for generating the third value based on input (first value) & output (second value) as output from the one shot device (Hsieh '800: Elements 104 or 102).

Hsieh '800 does not teach a method for modeling a bi-directional signal of an electrical circuit.

Mizoue '445 teaches method and system both for modeling the logical functions of a circuit (Mizoue '445:Abstract Lines 1-6).

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of Mizoue '445 to Hsieh '800 to store the value input/output/intermediate values of the simulated model. The motivation would have been that Mizoue '445 teaches a switch level simulator that works for bi-directional switches (Col.6, Lines 36-44) and Hsieh '800 is designing a bidirectional transfer system. Hence Mizoue '445 solves the modeling and capturing the input/intermediate/output state problem in Hsieh '800 model by modeling it through his simulator.

Regarding Claim 16 & 17

Methods for operation of improved pad cell model claims 16 & 17 disclose the same limitations as claim 1 and are rejected for the same reasons as claim 1.

Hsieh '800 does not teach a method for modeling/simulating a bi-directional signal of an electrical circuit.

Mizoue '445 teaches method and system both for modeling/simulating the logical functions of a circuit (Mizoue '445:Abstract Lines 1-6).

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of Mizoue '445 to Hsieh '800 to store the value input/output/intermediate values of the simulated model. The motivation would have been that Mizoue '445 teaches a switch level simulator that works for bi-directional switches (Col.6, Lines 36-44) and Hsieh '800 is designing a bidirectional transfer system. Hence Mizoue '445 solves the modeling and capturing the input/intermediate/output state problem in Hsieh '800 model by modeling it through his simulator.

8. **Claims 9-10, 13-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,428,800 issued to Wen-Jai Hsieh et al (Hsieh '800 hereafter) in view of U.S. Patent No. 4,922,445 issued to Yoshito Mizoue et al (Mizoue '445 hereafter), further in view of U.S. Patent No. 5,202,593 issued to Thomas B. Huang et al (Huang '593 hereafter).**

Regarding Claim 9

Hsieh '800 teaches a system for bi-directional signal transfer system (Hsieh '800: Abstract Lines 1-3; Col.2, Lines 26-28; Figure 4).

Mizoue '445 teaches a modeling and simulation system for logic design (Mizoue '445: Abstract).

Hsieh '800 & Mizoue '445 do not teach third value based on the resistor.

Huang '593 teaches generating third value based on resistive data (Huang '593: Figure 2: Element 102 to 110 to 104 (3rd output); Col.3 Lines 46-57), which according to the specification is derived from the pull up/pull down resistors/cells (Specification: Lines 24-27).

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of Mizoue '445 to Hsieh '800 to store the value input/output/intermediate values of the simulated model. The motivation would have been that Mizoue '445 teaches a switch level simulator that works for bi-directional switches (Col.6, Lines 36-44) and Hsieh '800 is designing a bidirectional transfer system. Hence Mizoue '445 solves the modeling and capturing

the input/intermediate/output state problem in Hsieh '800 model by modeling it through his simulator.

Further, It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of Huang '593 to Hsieh '800 to derive the third value based on the resistive data. The motivation would have been that since Hsieh '800 teaches using Huang '593 design (Col.1, Lines 19-20).

Further, It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to combine the teachings of Mizoue '445 to teachings of Huang '593 to simulate a model with delays included. The motivation would have been that Huang '593 teaches resistive load element (Huang '593: Figure 2) that can model the delay and Mizoue '445 model simulation accounts for such a delay between the input and the output (Mizoue '445: Col.4 Lines 8-19).

Regarding Claim 10

Teachings of Hsieh '800 are disclosed in the claim 8 rejection above.

Hsieh '800 does not teach simulating a bi-directional signal of a logic design.

Mizoue '445 teaches the simulating the logic design for set of known or unknown inputs for any logic circuit (Mizoue '445: Abstract Lines 1-6).

Motivation to combine Mizoue '445 with Hsieh '800 would be the same as disclosed in claim 8 rejection above.

Regarding Claim 13

Hsieh '800 teaches a system for bi-directional signal transfer system (Hsieh '800: Abstract Lines 1-3; Col.2, Lines 26-28; Figure 4).

Hsieh '800 does not teach a method of placing the input/output simulation result in the file.

Mizoue '445 teaches a method of placing the input data in the simulation file & placing the output data in simulation file (Mizoue '445: Col.4, Lines 64-68; Col5, Lines 1-7; Col.2, Lines 34-38, 50-59).

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of Mizoue '445 to Hsieh '800 to store the value input/output/intermediate values of the simulated model. The motivation would have been that Mizoue '445 teaches a switch level simulator that works for bi-directional switches (Col.6, Lines 36-44) and Hsieh '800 is designing a bidirectional transfer system. Hence Mizoue '445 solves the modeling and capturing the input/intermediate/output state problem in Hsieh '800 model by modeling it through his simulator.

Regarding Claim 14

Teachings of Hsieh '800 & Mizoue '445 are disclosed above in the claim 13 rejection.

Hsieh '800 & Mizoue '445 do not that is based on the resistive value associated with the bidirectional circuit.

Huang '593 teaches means of generating third value based on resistive data (Huang '593: Figure 2: Element 102 to 110 to 104 (3rd output); Col.3 Lines 46-57), which according to the specification is derived from the pull up/pull down resistors/cells (Specification: Lines 24-27).

Mizoue '445 teaches all the nodes - input, output, as well as the one inside the circuit are captured by the simulator (Mizoue '445: Col.5 Lines 54-61, Col.2, Lines 34-38, 50-59).

The motivation to combine these references towards and with each other is same as given above.

Regarding Claim 15

Hsieh '800 discloses a system with programmable bi-directional logic circuit, which can provide varied modes of operation (Hsieh '800: Col.1 Lines 65-68; Col.2 Lines 1-2). One of the disclosed mode is where at least two response values are provided. The mode is specifically embodied in Huang '593's implementation (Huang '593: Figure 1: Elements 12 & 14). Hsieh '800 teaches the second mode, where at least three response values are provided, namely, input output and the resolved (intermediate) values (Hsieh '800: Col.2 Lines 8-15).

Hsieh '800 & Huang '593 are not teaching simulation models of bidirectional logic circuit.

Mizoue '445 teaches a simulation model and result of such simulation can be used to capture all node values (Mizoue '445: Col.5 Lines 54-61, Col.2, Lines 34-38, 50-59).

The motivation to combine these references towards and with each other is same as given above.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 1-3, 8-10 and 13-17 are rejected under 35 U.S.C. 102(b) as being anticipated by SPICE Library & Users Manual (SPICE hereafter).

   SPICE teaches creating & editing models (SPICE: Chapter 4 creating and editing model) and provides library can be used and edited including components like transceivers, I/O Controllers, I/O ports, Bus, Bus Arbiters, Bus Controllers, UART, bridge drivers, transmission lines and transceiver interfaces (SPICE: Digital, Analog and Mixed Device Type Index). All these components inherently either model a bi-directional signal of an electrical circuit or can be modified easily to do so by the user manual teachings.

Remarks

10. All claims are rejected.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Akash Saxena whose telephone number is (571) 272-8351. The examiner can normally be reached on 8:30 - 5:00 PM M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jean R. Homere can be reached on (571)272-3780. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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